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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,319	11/24/2003	Hong-Gun Kim	5649-1182	9100

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EXAMINER
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GOUDREAU, GEORGE A

ART UNIT	PAPER NUMBER
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1763

DATE MAILED: 05/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/722,319

Applicant(s)

KIM ET AL.

Examiner

George A. Goudreau

Art Unit

1763

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 06 January 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-6,8-15,17-21,31-36,38 and 39 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 15,17,19-21,31, 33-36, and 38-39 is/are allowed.
- 6) ☒ Claim(s) 1-6,8-14,18 and 32 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

George A. Goudreau  
GEORGE GOUDREAU  
PRIMARY EXAMINER

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_

- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

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1. Applicant's arguments with respect to claims of record have been considered but are moot in view of the new ground(s) of rejection.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3-6, and 10-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamashita et. al. (JP 04-234,148).

Yamashita et. al. disclose a process for fabricating a device which is comprised of the following steps:

-A patterned Al wiring layer (3) is formed onto the surface of a gate oxide layer (2) on a Si wafer (1).;

-A PSG ILD (4) is conformably formed onto the surface of the wafer.;

-A SOG layer (5) is conformably formed onto the surface of the PSG ILD (4).;

-The SOG layer is baked at 125 C.;

-The baked SOG layer is etched back using a rie etching process.;

-The SOG layer is baked at 250 C.;

-The SOG layer is baked at 400 C.; and

-A PSG layer (6) is conformably formed onto the surface of the SOG layer (5).

This is discussed specifically in the abstract; and discussed in general in columns 1-12. This is shown in figures 1-13.

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4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 2, 8-9, and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over the reference as applied in paragraph 3 above.

The reference as applied in paragraph 3 above fail to disclose the following aspects of applicant's claimed invention:

- the specific cmp planarization of the top psg film after it has been formed onto the wafer in the process taught above;
- the specific means for forming the SOG film in the process taught above which are claimed by the applicant;
- the specific usage of an aqueous HF solution to etch back the SOG film in the process taught above; and

-the specific usage of a CVD process to form the psg film in the process taught above

It would have been obvious to one skilled in the art to cmp planarize the psg film which is formed in the process taught above based upon the following. It would have been desirable to flatten the psg film in the process taught above in order to facilitate the formation of a subsequently formed wiring layer, which is both flat, and level. This would desirably facilitate the vertical stacking of additional layers of circuitry on the wafer. Additionally, it would have been desirable to form subsequently formed layers of circuitry which are flat, and level since this type of circuitry would be less subject to delaminating during any subsequent thermal processing (i.e.-wave soldering of components, annealing, etc.) than other shapes of circuitry would be.

It would have been obvious to one skilled in the art to form the SOG layer in the process taught above using the specific means, which are taught by the applicant based upon the following. The usage of the specific means, which are claimed by the applicant for forming an SOG layer on the surface of a wafer, is conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.) Further, this would have simply represented the usage of an alternative, and at least equivalent means for forming an SOG layer on the surface of a wafer to the specific usage of other such means for do such.

It would have been obvious to one skilled in the art to form the PSG layer in the process taught above using the specific means, which are claimed by the applicant based upon the following. The usage of a CVD process to form a PSG film on the

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surface of a wafer is conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.) Further, this simply represents the usage of an alternative, and at least equivalent means for forming the PSG layer in the process taught above to the specific usage of other such means for doing such.

It would have been obvious to one skilled in the art to use an aqueous HF solution to etch back the SOG layer in the process taught above based upon the following. The usage of an aqueous HF solution to wet etch a SOG layer is conventional or at least well known in the semiconductor processing arts. (The examiner takes official notice in this regard.) Further, this simply represents an alternative, and at least equivalent means for etching back the SOG layer in the process taught above to the specific means, which are taught above.

7. Claims 1-6, 8-14, 18, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over the reference as applied in paragraph 5 of the previous office action further in view of Yamashita et. al. (JP 04-234,148).

The reference as applied in paragraph 5 of the previous office action fail to specifically disclose the specific SOG baking temperatures, which are claimed by the applicant.

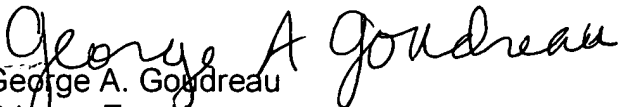
Yamashita et. al. teach that it is desirable to soft bake an SOG which has deposited onto the surface of a wafer at an initial temperature of 125 C.

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It would have been obvious to one skilled in the art to soft bake the SOG layer in the process taught above at 125 C based upon the teachings of Yamashita et. al. that it is desirable to do such.

8. Claims 15, 17, 19-21, 31, 33-36, and 38-39 are allowed.
9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
10. This action will not be made final due to the new grounds of rejection.
11. Any inquiry concerning this communication should be directed to examiner

George A. Goudreau at telephone number (571)-272-1434.

  
George A. Goudreau  
Primary Examiner  
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